REMARKS

Claims 1-6 and 9 are pending in this application. Claim 1 has been amended to incorporate the subject matter of claim 7, which has been canceled. The amendments are fully supported by the specification as originally filed (see, e.g., page 5, lines 11-14 of specification).

Applicant's invention is directed to a semiconductor package, including: a substrate having a first surface disposed with a plurality of conductive traces and a second surface disposed with a plurality of electrical connection terminals; at least a chip and a passive device formed on the first surface of the substrate and electrically connected to the conductive traces; and a flash-proof device having an outer sidewall aligned with a side edge of the substrate, the flash-proof device being attached to the first side of the substrate, such that the chip and passive device are received in a cavity of the flash-proof device. Also, as recited in claim 1, a distance in elevation from a top side of the flash-proof device to the first side of the substrate is slightly greater than a depth of a molding cavity of an encapsulation mold used in a molding process.

During molding, the substrate can be tightly clamped between the flash-proof device and the encapsulation mold, where the top side of the flash-proof device abuts against an upper mold. As such, a second side of the substrate hermetically abuts against a lower mold. Based on the claimed elevation-to-depth arrangement of the flash-proof device and the molding cavity, the molding compound will encapsulate the chip and passive device, while leaving the top side of the flash-proof device and the second side of the substrate exposed to outside the encapsulant, such that the second side of the substrate is **free of flash** of the molding compound.

Claims 1, 3, 4, and 6 were rejected under 35 USC 103(a) as being unpatentable over "AAPA" in view of U.S. Patent 6,191,360 to Tao et al. (hereinafter "Tao"). Claim 2 was rejected under 35 USC 103(a) as being unpatentable over "AAPA" in view of Tao, and further in view of U.S. Patent 5,812,570 to Spaeth. Claim 5 was rejected under 35 USC 103(a) as being unpatentable over "AAPA" in view of Tao, and further in view of U.S. Patent 5,530,295 to Mehr. Claim 7 was rejected under 35 USC 103(a) as being unpatentable over "AAPA" in view of Tao, and further in view of U.S. Patent 6,294,831 to Shishido et al. Claim 9 was rejected under 35

USC 103(a) as being unpatentable over "AAPA" in view of Tao, and further in view of U.S. Patent 6,392,900 to Petty et al. These rejections are respectfully traversed.

As stated on page 2 of the Office Action: "AAPA fails to disclose a flash proof device attached to the first side of the substrate."

In the Office Action, Tao was cited to remedy this deficiency by providing a heat spreader 34 that is attached to a substrate. However, Tao does not teach or suggest that a distance in elevation from a top side of the heat spreader 34 to the first side of the substrate 30 is slightly greater than a depth of a molding cavity of a mold. Instead, the figures in Tao suggest that the depth of the molding cavity is equal to or greater than the distance between the top side of the heat spreader 34 and the first side of the substrate 30. There is no teaching or suggestion in Tao that the depth of the molding cavity should be smaller than the distance in elevation between the top side of the heat spreader 34 and the first side of the substrate 30.

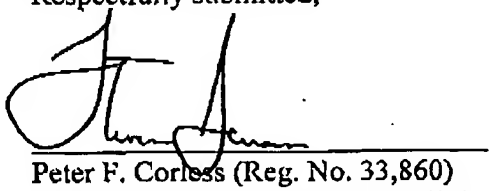
Thus, even if the heat spreader of Tao were somehow incorporated into the semiconductor package of "AAPA," this arrangement would not be sufficient to prevent molding resin from flashing over the second surface of the substrate.

Moreover, the heat spreader 34 of Tao clearly does not have an outer sidewall aligned with a side edge of the substrate, as recited in claim 1. According to the Applicant's invention, an outer sidewall 241 of the flash-proof device 24 is aligned with a side edge 204 of the substrate 20 to maximize the surface area on the first side 200 of the substrate 20 for holding chips and passive devices (see specification at page 5, lines 11-14). Even if "AAPA" were somehow combined with Tao, the combination would fail to teach or suggest at least this feature of the Applicant's claimed invention. For at least the reasons discussed above, claim 1 and dependent claims 2-6 and 9 patentably distinguish over the combination of "AAPA" in view of Tao. The other cited references (Spaeth, Mehr, Shishido, and Petty) similarly fail to teach or suggest at least the above-described features of the Applicant's claimed invention.

For example, Shishido does not teach or suggest a flash-proof device formed with a cavity for receiving a chip and passive device, where the flash-proof device has an outer sidewall aligned with a side edge of the substrate. In FIG. 1 of Shishido, the thermally conductive structure 18 includes an open portion 26 for receiving a semiconductor chip 14, but there is no teaching or suggestion of receiving one or more chips **and** passive devices in the open portion, as recited in claim 1. Shishido is designed to accommodate only a single semiconductor chip, and would not be capable of containing one or more additional chips and/or passive devices. Moreover, the package structure taught in Shishido does not include an encapsulant, and thus is a different type of package that could not be combined with "AAPA" and/or Tao to somehow produce the Applicant's claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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